PNX0161

PNX0161 personal audio IC

Rev. 01 — 17 January 2008 Product data sheet

1. Introduction

The Nexperia PNX0161 is an integrated IC that serves as USB audio and HID class device for a USB headset.

2. General description

Recent development in mobile phones is to have the phone equipped with a USB micro A plug as a single plug for charging and connection to all enhancements (like a headset, but also for other enhancements like GPS accessories etc.)

The PNX0161 is based on an ARM7TDMI CPU core with data/instruction cache of 8 kB and USB 2.0 FS device interface.

3. Features

3.1 General features

- Enables one chip solution for USB headset.
- Requires very low power.
- Supports FM radio input including low-power audio bypass mode.
- Is available in a small footprint package TFBGA88 of 7 × 7 sq. mm with 0.5 mm pitch.

3.2 Hardware features

- ARM7TDMI processor core with 8 kB data/instruction cache.
- Embedded SRAM, 32 kB.
- Embedded ROM memory for storing the boot code, 32 kB.
- Embedded flash memory for storing the program code, 256 kB (second production version will be ROM based).
- Integrated USB 2.0 full-speed device interface.
- Intelligent configuration power management.
- Embedded high-efficiency power supply unit powered from a USB supply.
- Supports power optimization by optimizing supply voltages.
- Embedded DMA controller.
- Digital interfaces:
  - Integrated stereo ADC with programmable amplifier (microphone, line input and tuner input).
  - Integrated IIS input and output interfaces (configurable for master/slave options).
  - Integrated fast UART with DMA support.

- Integrated master/slave I^2C interface.

- Analog interfaces:
  - Integrated stereo ADC with programmable amplifier (microphone, line input and tuner input).
  - Microphone bias block.
  - Integrated stereo DAC with Class-AB headphone amplifier for high quality audio with increased driving capabilities and for use in tuner applications.
  - The integrated ADC and DAC both have a 24 bits data path.
- Two integrated general purpose timers.
- Integrated watchdog timer.
- Low-power tuner mode with direct connection between tuner input and Class-AB headphone amplifier with analog volume control.
- JTAG interface with boundary scan and ARM debug access.

3.3 Software features

This section lists the software features that the PNX0161 is capable of performing.

- Playback: playback by the headphones of a received USB audio stream from the USB host via the DAC.
- Recording: audio stream converted by the ADC from the microphone is sent via the USB audio stream to the USB host.
- Phone call: in addition to the first case, simultaneously returning a USB audio stream that is converted by the ADC from the microphone. The microphone is mixed to the headphone stream, known as side-tone mixing.
- Tuner listening: the FM tuner audio stream is sent to the headphones. No stream is sent or received via USB.
- Tuner recording: the FM tuner audio stream is sent to the headphones. In addition the FM tuner stream is streamed to the phone via USB.
- USB HID class for FM tuner RDS info.
- USB device firmware upgrade.
- Intelligent power management software.
- Audio postprocessing features like volume control.

3.4 Software features on request

This section lists the software features that the PNX0161 is capable of performing.

- Audio source selection between line-in and USB audio in for playback path, by toggling GPIO pin.
- Support for stereo recording from analog and I^2S inputs at sample rates other than 48 kHz.
- Support for stereo playback from USB audio, I^2S and analog inputs at sample rates other than 48 kHz.
- Option for a “direct analog link” for playback applications where only volume control is performed in the PNX0161. The “direct analog link” provides a full analog audio path through the PNX0161 from the analog stereo line input to the low output impedance buffer output through an analog volume control block. When the option is not selected, the analog stereo input is converted to the digital domain by the on-chip ADC. Audio

postprocessing is performed in the digital domain. The processed signals are then converted back to analog by the on-chip DAC and fed to the analog outputs through the low impedance output buffer.

- Digital EQ for loudspeaker characteristics compensation.
- For audio rendering applications: digital bass boost, treble expander, stereo widening, FM radio acoustical performance improvement and other NXP software LifeVibes music algorithms.
- For applications as USB (mobile)-phones hands-free teleconference stations: Full duplex acoustic echo cancellation, intelligibility improvement and other NXP software LifeVibes voice algorithms.

4. Applications

- USB headset
- FM radio USB headset
- Docking station

5. Ordering information

Table 1. Ordering information

Type numbers	Package		
	Name	Description	Version
PNX0161ET/N101	TFBGA88	TFBGA88: plastic thin fine-pitch ball grid array package; 88 balls; body 7 x 7 x 0.8 mm	SOT951-1

6. Marking

Table 2. Marking codes

Lines	Digits	Comments
A	0161ET/01	Commercial name
B	Diffusion batch ID /wafer ID Assy sequence ID	DBID and ASID
C	ZPDYYWW1X	Z = Fab. Location (SSMC) P = Assembly Factory (APC) D = Green product meeting RoHS (Lead and Halogen free) YYWW = date code 1 version = N1 version X = development status code (will change to ‘Y’ for production.)

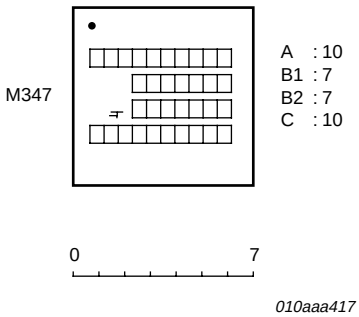


Fig 1. PNX0161 marking

7. Block diagram

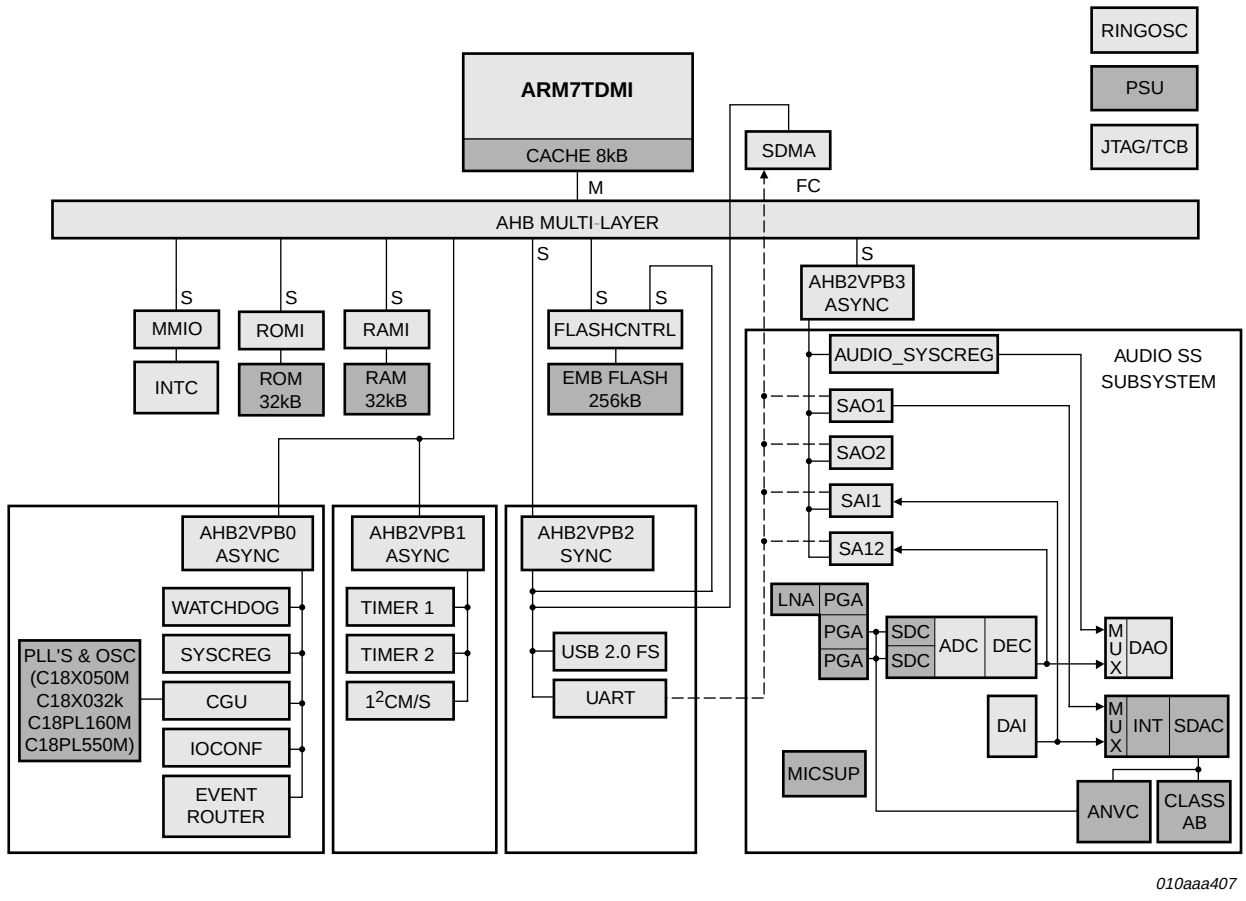


Fig 2. PNX0161 block diagram

8. Pinning information

8.1 Pinning

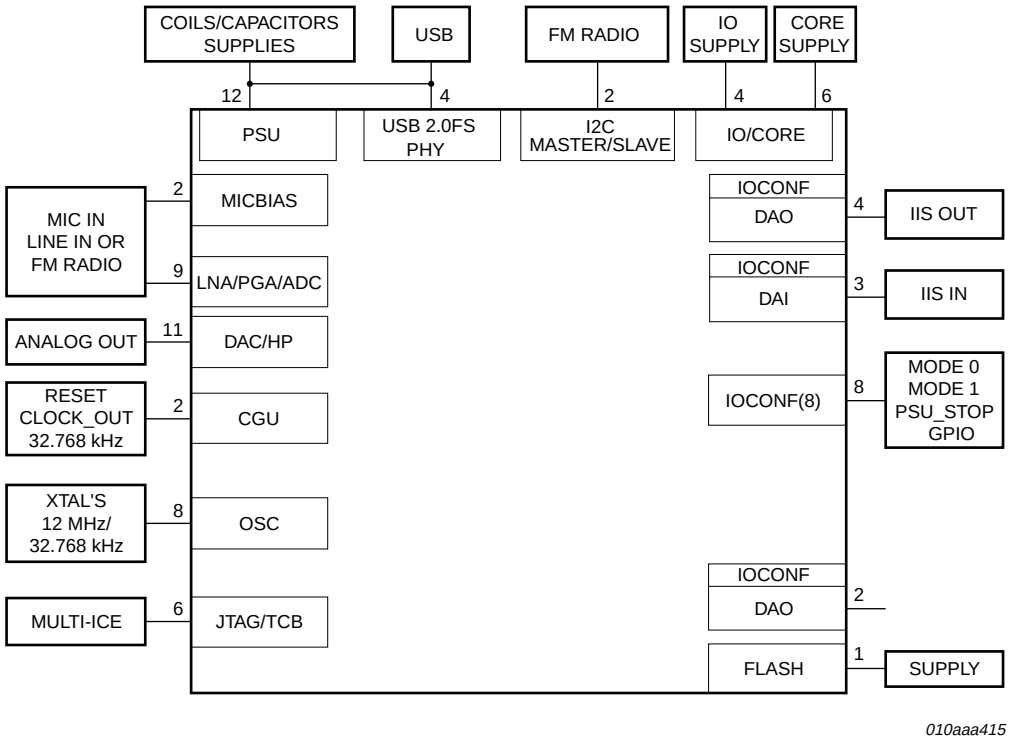


Fig 3. PNX0161 pin configuration diagram

Table 3. Pinning list

BGA pin name	GPIO	BGA ball	Digital I/O level	Application function	Pin state after reset	Cell type[1]	Description
12 MHz oscillator (fixed 4 pins)							
XTALH_IN	-	J1	-	analog	input	apio (Z)	12 MHz clock input
XTALH_OUT	-	H1	-	analog	output	apio (IO)	12 MHz clock output
XTALH_VDDA18	-	H2	SUP2	-	-	vddco	Analog supply oscillators
XTALH_VSSA	-	K2	-	-	-	vssco	Analog ground oscillators
32.768 kHz oscillator (fixed 4 pins)							
XTALL_IN	-	G1	-	analog	input	apio (Z)	32.768 kHz clock input
XTALL_OUT	-	F1	-	analog	output	apio (IO)	32.768 kHz clock output
XTALL_VDDA18	-	E2	SUP2	-	-	vddco	Analog supply oscillators/PLLs
XTALL_GNDA	-	G2	-	-	-	vssco	Analog ground oscillators/PLLs
I^2C (fixed 2 pins)							

Table 3. Pinning list *…continued*

BGA pin name	GPIO	BGA ball	Digital I/O level	Application function	Pin state after reset	Cell type[1]	Description
I2C_SDA	-	C13	0-5 VDC tolerant	input/output	input	iic3m4sdat5v	Serial data I^2C
I2C_SCL	-	C12	0-5 VDC tolerant	input/output	input	iic3m4sdat5v	Serial data I^2C
USB interface (fixed 4 pins)							
USB_VBUS	-	A13	SUP1	-	input	bpts5ptpht5v	USB supply detection
USB_CONNECT_N	-	B13	0-5 VDC tolerant	-	output	bpts5ptpht5v	Soft connect output USB 2.0 FS
USB_DP	-	A12	-	-	input	usb 11f1	Positive USB data line
USB_DM	-	A11	-	-	input	usb 11f1	Negative USB data line
PSU (fixed 12 pins)							
PSU_VBUSA	-	N9	SUP1	analog	-	vddcobf	USB supply voltage
PSU_VBUSB	-	N12	SUP1	analog	-	vddcobf	USB supply voltage
PSU_VOUT33	-	M13	SUP3	-	-	vddcobf	DCDC1 3.3 V output voltage
PSU_LX_VOUT33	-	N10	-	-	-	vddco	Connection to DCDC1 external coil (PSU_LX1)
PSU_VSS1	-	M9	-	-	-	vssco	Ground for DCDC1 Nswitch (no substrate)
PSU_VSS2	-	M10	-	-	-	vssco	Ground for DCDC2 Nswitch (no substrate)
PSU_LX_VOUT14	-	N11	-	analog	-	vddco	Connection to DCDC2 3 external coil (PSU_LX2)
PSU_VOUT14	-	N13	SUP2	-	-	vddcobf	DCDC1 1.4 V output voltage
PSU_CLEAN	-	L12	-	-	-	vssco	Reference circuit ground not connected to substrate
PSU_GND	-	M11	-	-	-	vssco	Core ground and substrate
PSU_PLAY	-	L13	-	analog	-	apio	Play button input
PSU_STOP	-	K13	-	analog	-	apio	Stop button input
GPIO (fixed 8 pins)							
GPIO_0	Yes	J13	0-5 VDC tolerant	input/output	input	bpts5ptpht5v	General purpose IO pin MODE0 (pull-down)[2]
GPIO_1	Yes	G12	0-5 VDC tolerant	input/output	input	bpts5ptpht5v	General purpose IO pin MODE1 (pull-down)[3]
GPIO_2	Yes	H13	0-5 VDC tolerant	input/output	input	bpts5ptpht5v	General purpose IO pin STOP
GPIO_3	Yes	G13	0-5 VDC tolerant	input/output	input	bpts5ptpht5v	General purpose IO pin
GPIO_4	Yes	H12	0-5 VDC tolerant	input/output	input	bpts5ptpht5v	General purpose IO pin

Table 3. Pinning list *…continued*

BGA pin name	GPIO	BGA ball	Digital I/O level	Application function	Pin state after reset	Cell type[1]	Description
GPIO_5	Yes	F13	0-5 VDC tolerant	input/output	input	bpts5ptpht5v	General purpose IO pin
GPIO_6	Yes	F12	0-5 VDC tolerant	input/output	input	bpts5ptpht5v	General purpose IO pin
GPIO_7	Yes	E13	0-5 VDC tolerant	input/output	input	bpts5ptpht5v	General purpose IO pin
DAI (fixed 3 pins)							
DAI_DATA	Yes	N1	0-5 VDC tolerant	input/output	input (GPIO)	bpts5ptpht5v	I^2S in data
DAI_WS	Yes	N4	0-5 VDC tolerant	input/output	input (GPIO)	bpts5ptpht5v	I^2S in wordselect
DAI_BCK	Yes	N6	0-5 VDC tolerant	input/output	input (GPIO)	bpts5ptpht5v	I^2S in bit clock
DAO (fixed 4 pins)							
DAO_DATA	Yes	N7	0-5 VDC tolerant	input/output	input (GPIO)	bpts5ptpht5v	I^2S out data
DAO_WS	Yes	M7	0-5 VDC tolerant	input/output	input (GPIO)	bpts5ptpht5v	I^2S out wordselect
DAO_BCK	Yes	M6	0-5 VDC tolerant	input/output	input (GPIO)	bpts5ptpht5v	I^2S out bit clock
DAO_CLK	Yes	N5	0-5 VDC tolerant	input/output	input (GPIO)	bpts5ptpht5v	I^2S out clock 256 FS
UART (fixed 2 pins)							
UART_TXD	Yes	K12	0-5 VDC tolerant	input/output	input (GPIO)	bpts5ptpht5v	Serial output
UART_RXD	Yes	J12	0-5 VDC tolerant	input/output	input (GPIO)	bpts5ptpht5v	Serial input[4]
CGU (fixed 2 pins)							
RSTN_IN	-	K1	0-5 VDC tolerant	input	input	bpts5ptpht5v	System reset input (active low pull-up)
CLK_OUT	Yes	J2	0-5 VDC tolerant	input/output	output	bpts5ptpht5v	32.768 kHz clock output
Embedded flash (fixed 1 pin)							
FLASH_VDD_HV	-	E12	SUP2	-	-	vddco	Supply
NA	-	Not visible on package	-	-	-	bpts5ptpht5v	Duty cycle measurement
-	-	Not visible on package	-	-	-	bpts5ptpht5v	Address count up (pull-down)
-	-	Not visible on package	-	-	-	apio (IO)	Sense amp trip point

Table 3. Pinning list *…continued*

BGA pin name	GPIO	BGA ball	Digital I/O level	Application function	Pin state after reset	Cell type[1]	Description
-	-	Not visible on package	-	-	-	apio (ZI)	Measure trip point current for sense amps
-	-	Not visible on package	-	-	-	bpts5ptpht5v	Overrule write and erase security and protections (pull-down)
-	-	Not visible on package	-	-	-	VPEX	Observe or supply positive write/erase voltage (11.5 V)
-	-	Not visible on package	-	-	-	VNEX	Observe or supply negative write/erase voltage (5.5 V)
DAC/HP (fixed 11 pins)							
DAC_VDDA33	-	B10	SUP3	-	-	vddco	SDAC analog supply
DAC_VREFP	-	A9	AI	-	-	apio	SDAC positive reference voltage
DAC_VREFN	-	B9	AI	-	-	apio	SDAC negative reference voltage
HP_OUTL	-	A5	AO	-	-	apio	Headphone left output
HP_OUTR	-	A7	AO	-	-	apio	Headphone right output
HP_FCL	-	B5	AI	-	-	apio	Headphone filter capacitor left
HP_FCR	-	A8	AI	-	-	apio	Headphone filter capacitor right
HP_VDDA33	-	B6	Supply	-	-	vddco	Headphone analog supply class-AB
	-	B6	Supply	-	-	vddco	Double bonding
HP_GNDA	-	B7	Ground	-	-	vssco	Headphone analog ground
	-	B7	Ground	-	-	vssco	Double bonding
HP_OUTC	-	A6	AO	-	-	apio	Headphone common output reference Class-AB
	-	-	AO	-	-	apio	-
HP_VREF	-	B8	AI	-	-	apio	Analog reference supply For headphone and DAC
ADC/MIC (fixed 9 pins)							
ADC_MIC	-	A4	AI	-	-	apio	ADC microphone input
ADC_VINL	-	A2	AI	-	-	apio	ADC line input left
ADC_VINR	-	A1	AI	-	-	apio	ADC line input right
ADC_VREF	-	B1	AO	-	-	apio	ADC reference voltage output
ADC_VREFN	-	C2	AI	-	-	apio	ADC negative reference voltage

Table 3. Pinning list *…continued*

BGA pin name	GPIO	BGA ball	Digital I/O level	Application function	Pin state after reset	Cell type[1]	Description
ADC_VREFP	-	A3	AI	-	-	apio	ADC positive reference voltage
ADC_VDDA18	-	D1	Supply	-	-	vddco	ADC digital voltage supply
ADC_VDDA33	-	C1	Supply	-	-	vddco	ADC analog voltage supply
ADC_GNDA	-	D2	Ground	-	-	vssco	ADC analog ground
MicSUP (fixed 2 pins)							
MIC_VREFSUP	-	B4	AI	-	-	apio	MIC clean reference voltage
MIC_OUTSUP	-	B3	AO	-	-	apio	MIC supply voltage
Debugging (fixed 6 pins)							
JTAGSEL_ARM	-	M3	0-5 VDC tolerant	input	input	bpts5ptpht5v	JTAG selection ARM (pull-down)
JTAG_TDI	-	M4	0-5 VDC tolerant	input	input	bpts5ptpht5v	JTAG data input (pull-up)
JTAG_TCK	-	N2	0-5 VDC tolerant	input	input	bpts5ptpht5v	JTAG clock input (pull-up)
JTAG_TMS	-	N3	0-5 VDC tolerant	input	input	bpts5ptpht5v	JTAG mode select input (pull-up)
JTAG_TRST_N	-	M1	0-5 VDC tolerant	input	input	bpts5ptpht5v	JTAG reset input (pull-down)
JTAG_TDO	-	M5	0-5 VDC tolerant	input/output	output	bpts5ptpht5v	JTAG data output
Supplies (fixed 10 pins)							
VDDE0	-	E1	SUP3	-	-	vdde3v3	Peripheral supply
VSSE0	-	F2	-	-	-	vsse3v3	Peripheral ground
VDDE1	-	N8	SUP3	-	-	vdde3v3	Peripheral supply
VSSE1	-	M8	-	-	-	vsse3v3	Peripheral ground
VDDE2	-	D13	SUP3	-	-	vdde3v3	Peripheral supply
VSSE2	-	D12	-	-	-	vsse3v3	Peripheral ground
VDDI0	-	L1	SUP2	-	-	vddco	Core supply
VSSI0	-	L2	-	-	-	vssco	Core ground
VDDI1	-	A10	SUP2	-	-	vddco	Core supply
VSSI1	-	B11	-	-	-	vssco	Core ground
Unused BGA balls (4 pins)							
Not used	-	B2	-	-	-	-	-
Not used	-	B12	-	-	-	-	-
Not used	-	M2	-	-	-	-	-
Not used	-	M12	-	-	-	-	-

[1] Cell types are explained in Table 5.

[2] GPIO0 is a bootstrap MODE pin, for further details see application note on PNX0161.

[3] GPIO1 is a bootstrap MODE pin, for further details see application note on PNX0161.

[4] UART_TX is a bootstrap MODE pin, for further details see application note on PNX0161.

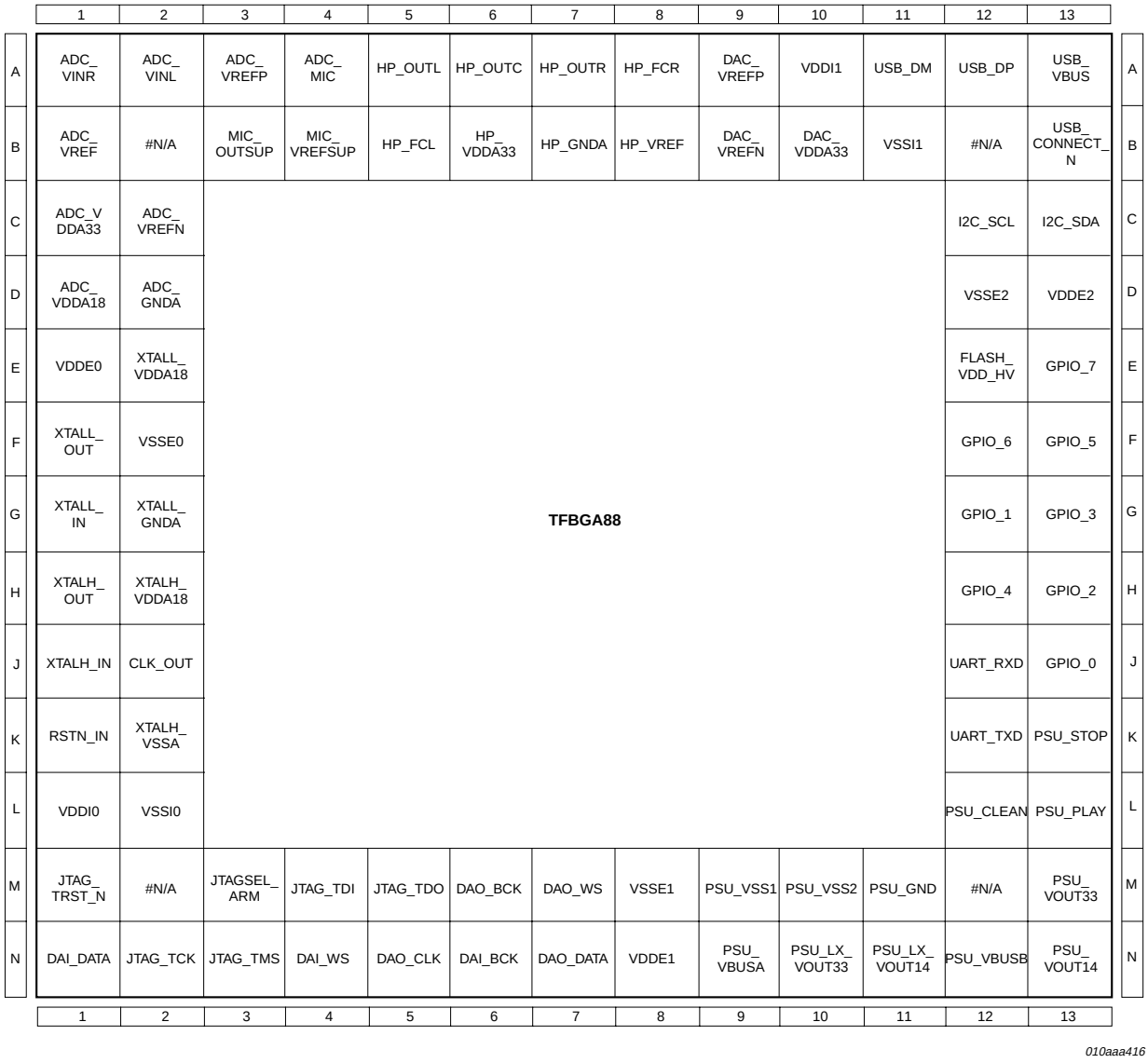


Fig 4. Pinning diagram

Table 4. Supply domains

Supply domain	Typical voltage (V)	Related supply pins	Description
SUP2	1.4 - 1.8	VDDI0, VDDI1, VDDA18	Core supply
SUP3	3.0 - 3.3	VDDE0, VDDE1, VDDE2, ADC_VDDA33, DAC_VDDA33, HP_VDDA33	Peripheral and analog supplies
SUP1	4.0 - 5.25	PSU_VBUS	USB V_{BUS} voltage

Table 5. Cell types

Library name[1]	Function	Description
bpts5ptpht5v	Digital input/output	Bidirectional pad; plain input; 3-state output; SSO control; CMOS with programmable hysteresis and repeater.
bpts5ptpht5v	Digital input/output	IIC cell; clock signal; cell based ESD protection.
apio	Analog input/output	Analog pad; analog input/output.
vddco	Core supply	-
vddcobf	Core supply	-
vddco*	Core supply	An adapted VDDCO pad from library with the following modification: • Removing the capacitive coupled gate triggering of the gcNMOST protection between pad and substrate. • Connect the gate to substrate. • Add a P-diode between ggNMOST and pad. • Add a N-diode between pad and substrate.
vddi	Core supply	-
vdde3v3	Peripheral supply	-
vssco	Core ground	-
vssis	Core ground	-
vsse3v3	Peripheral ground	-

[1] The library name is the official name of the cell in the CMOS library. To increase readability, nicknames for the cells have been created for this document. Throughout this document, the nickname is used to refer to a certain cell type instead of its official name.

9. Limiting values

Table 6. Limiting values

In accordance with the absolute maximum rating system (IEC 134)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
All digital I/Os						
V_I	input voltage	-	–0.5	-	+5.0	V
V_O	output voltage	-	–0.5	-	+3.6	V
I_O	output current	$V_{DD(EXT)}$ = 3.3 V	-	4	-	mA
Temperature values						
T_j	junction temperature	-	0	-	125	°C
T_{stg}	storage temperature	-	–40	-	+85	°C
T_{amb}	ambient temperature	-	–15	+25	+70	°C
Electrostatic handling						
V_{ESD}	electrostatic discharge voltage	HBM, human body mode	–2000	-	+2000	V
		CDM, charge, device mode	-	500	-	V

10. Static characteristics

This chapter gives an overview of the most important static characteristics of the PNX0161. More detailed specifications will be given in future versions of this document.

Table 7. Static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(EXT)}$	external supply voltage	<0,2 >	3.0	3.3	3.6	V
$V_{DD(INT)}$	internal supply voltage	<0..1 >	1.3	1.4	1.95	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)	12 MHz XTAL osc/PLL	1.3	1.4	1.95	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		3.0	3.3	3.6	V
V_{BUS}	bus supply voltage		4.0	5.0	5.25	V

Table 8. Power supply unit static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{O(VBUS)}$	V_{BUS} output power	-	4.0	5	5.25	V
$V_{O(3V3)}$	output voltage (3.3 V)	-	2.4	3.0	3.2	V
$\Delta V_{O(3V3)}$	output voltage variation (3.3 V)	-	–50	-	+50	mV
$V_{O(1V4)}$	output voltage (1.4 V)	-	1.3	1.4	1.95	V
$\Delta V_{O(1V4)}$	output voltage variation (1.4 V)	-	–50	-	+50	mV
$I_{O(3V3)}$	output current (3.3 V)	-	-	-	50	mA
$I_{O(1V4)}$	output current (1.4 V)	-	-	-	50	mA
$\eta_{DCDC(33)}$	DC-to-DC converter efficiency (33 %)	-	-	85	-	%
$\eta_{DCDC(14)}$	DC-to-DC converter efficiency (14 %)	-	-	81	-	%
f_{clk}	clock frequency	-	-	12	-	MHz
f_{osc}	oscillator frequency	-	8	10	12	MHz
f_{sw}	switching frequency	-	-	1	-	MHZ

Table 9. Analog in - electrical parameters DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA(ADC)(3V3)}$	ADC analog supply current (3.3 V)	-	-	2.2	-	mA
$I_{DDA(ADC)(1V8)}$	ADC analog supply current (1.8 V)	-	-	-	20	mA
$I_{ref(neg)}$	negative reference current	-	-	20	-	µA
$I_{ref(pos)}$	positive reference current	-	-	20	-	µA
$I_{DDA(SDC)}$	SDC analog supply current	-	-	0.4	-	mA
$I_{DDA(PGA)}$	PGA analog supply current	-	-	430	-	µA
G_{PGA}	PGA gain	-	-	–1.94	-	dB
$I_{DDA(bias)}$	bias analog supply current	N = 13 for all modules on	-	190 + N*10	-	µA
$I_{DDA(LNA)}$	LNA analog supply current	-	-	0.85	1.2	mA

Table 9. Analog in - electrical parameters DC characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_{LNA}	LNA gain	in a bandwidth between 300 Hz and 5 kHz.	28	30	32	dB
R_{ref}	reference resistance	headphone and DAC	-	11.25	-	kΩ
R_{com}	common resistance	headphone	-	11.25	-	kΩ
ΔG	gain mismatch	-	0	-	24	dB

11. Dynamic characteristics

This chapter shows the audio performance characteristics of the PNX0161. A more extensive list of dynamic characteristics will be given in future versions of this document.

Table 10. Timing and other characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
12 MHz oscillator (XTALH)						
f_{osc}	oscillator frequency	-	-	12	-	MHz
δ	duty cycle	-	-	50	-	%
C_i	input capacitance	-	-	-	2	pF
C_o	output capacitance	-	-	-	0.74	pF
t_{start}	start time	-	-	500	-	µs
P	power dissipation	crystal level of drive	100	-	500	µW

Table 11. Dynamic characteristics of Class AB amplifier at 3.0 V - DC mode[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage	HP unloaded	-	830	-	mV_{RMS}
P_o	output power	R_L = 32 Ω	-	-	2.5	mW
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	(measured with 20 kHz block filter) at 0 dBFS, f_i = 1 kHz, R_L = 32 Ω	-	–59	-	dB
		at –60 dBFS, f_i = 1 kHz, R_L = 32 Ω	-	–35	–30	dBA
S/N	signal-to-noise ratio	HP unloaded (measured with 20 kHz block filter)	-	96	-	dBA
α_{ripple}	ripple rejection	R_L = 32 Ω	-	6	-	dB
α_{ct}	crosstalk attenuation	at 0 dBFS, f_i = 1 kHz, R_L = 32 Ω	-	–42	-	dB

[1] T_{amb} = 25 °C; unless otherwise specified.

Table 12. Analog in - electrical parameters AC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
B	bandwidth	at 48 kHz sampling rate	-	-	21.7	kHz
THD	total harmonic distortion	THD+N @ 0 dBFS; f_i = 1 kHz tuner, line input level = 1 V, PGA setting 0 dB	-	–73	-	dB
		THD+N @ –60 dBFS; f_i = 1 kHz; A-weighted tuner, line imputatively = 1 mV, PGA setting 0 dB	-	30	-	dBA
S/N	signal-to-noise ratio	tuner, line imputatively = 1 V, PGA setting 0 dB; A-weighted	-	90	-	dBA
Z_i	input impedance	line in/tuner mode	-	12	-	kΩ

Table 12. Analog in - electrical parameters AC characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Microphone						
THD	total harmonic distortion	THD+N @ 0 dBFS V_i mic = 20 µV; f_i = 1 kHz	-	–70	-	dB
		THD+N @ –60 dBFS; A-weighted V_i mic = 20 µV; f_i = 1 kHz	-	31	-	dBA
Z_i	input impedance	-	-	5	-	kΩ

Table 13. Digital - electrical parameters AC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ARM}	ARM frequency	-	-	-	48	MHz

Table 14. Power figures

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{stb(susp)}$	suspend mode standby current	-	-	750	-	µA
P	power dissipation	playback: by the headphones of a received USB audio stream from USB host via the DAC. • V_{bus} = 5 V • $V_{O(1V4)}$ = 1.46 V • $V_{O(3V3)}$ = 3.0 V DC-coupled (HP 32 Ω) output power adjusted to 0,5 mW using 1 kHz sine wave. normalized test MP3 file is used, tin arena, chains. playback volume: maximum volume in volume control, Vol = 35 in media player	-	45	-	mW
		recording: audio stream converted by the ADC from the microphone is sent via USB audio stream to the USB host. • V_{bus} = 5 V • $V_{O(1V4)}$ = 1.46 V • $V_{O(3V3)}$ = 3.0 V	-	53	-	mW

Table 14. Power figures *…continued*

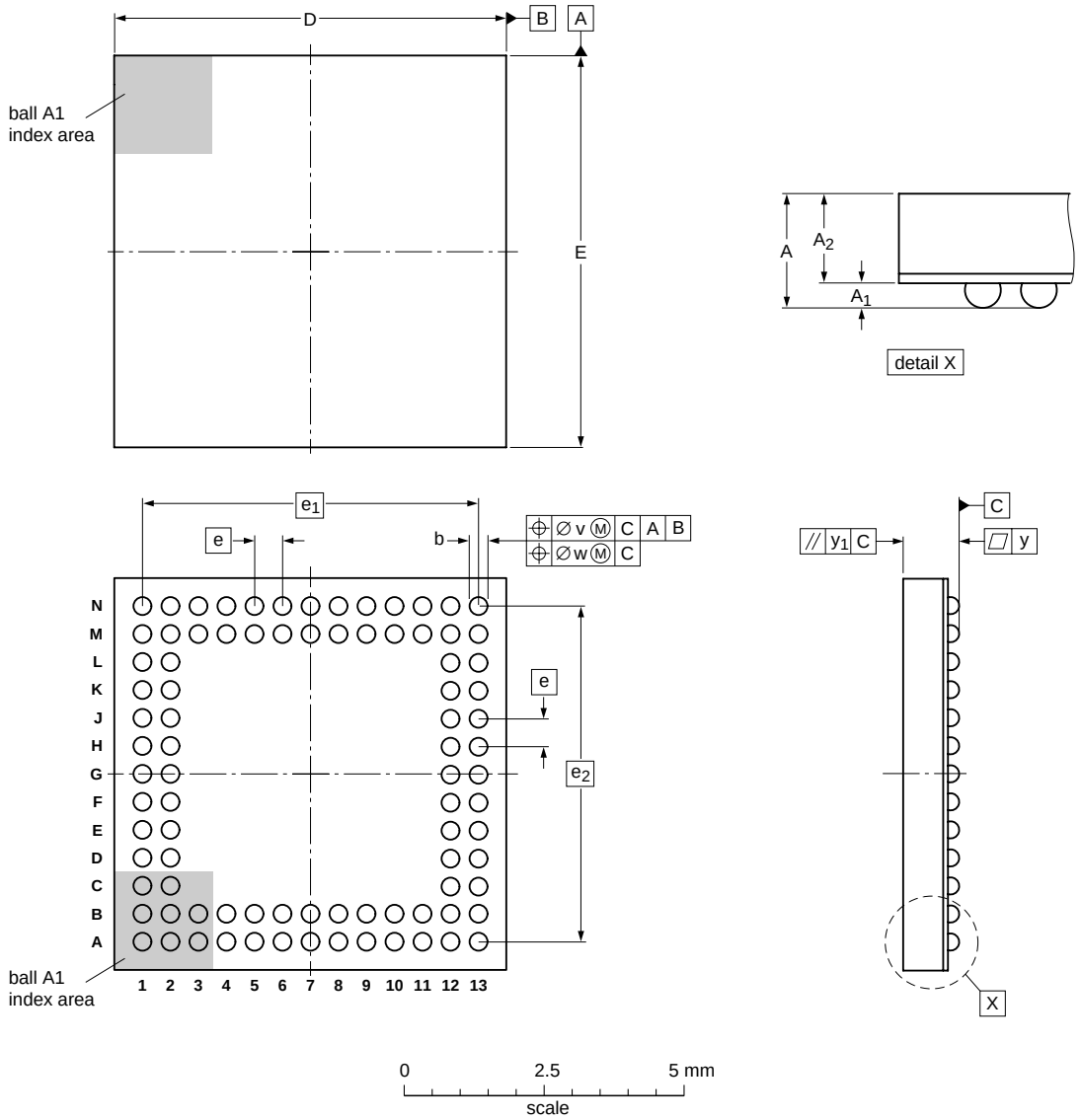
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P	power dissipation	phone call: in addition to the first case, simultaneously returning a USB audio stream that is converted by the ADC from the microphone. The microphone is mixed to the headphone stream, known as side-tone mixing. • V_{bus} = 5 V • $V_{O(1V4)}$ = 1.46 V • $V_{O(3V3)}$ = 3.0 V DC-coupled (HP 32 Ω).	-	72	-	mW
		tuner listening: the FM tuner audio stream is sent to the headphones. No stream is sent or received via USB.	-	80	-	mW
		tuner recording: the FM tuner audio stream is sent to the headphones. In addition the FM tuner stream is streamed to the phone via USB. THD+N @ 0 dBFS; f_i = 1 kHz.	-	117	-	mW
P_{max}	maximum power dissipation	phone UC + max freq SYSBASE at 48 MHz and MAX volume.	-	172	-	mW

Table 15. DFU downloading

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{bit(UHCI)}$	UHCI bit rate	limited by a USB control end point size of 8 bytes measured with 2 kB transfer.	-	8	-	kB
$f_{bit(OHCI)}$	OHCI bit rate	2 kB transfer	-	77	-	kB

12. Package outline

TFBGA88: plastic thin fine-pitch ball grid array package; 88 balls; body 7 x 7 x 0.8 mm **SOT951-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.1	0.25 0.15	0.85 0.75	0.35 0.25	7.1 6.9	7.1 6.9	0.5	6	6	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT951-1	- - -	MO-195	- - -			~~06-05-26~~ 06-08-25

Fig 5. Package outline SOT951-1 (TFBGA88)

13. Abbreviations

Table 16. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
ADSS	AuDio SubSystem
AHB	Advanced Peripheral Bus
AVC	Analog Volume Control
CGU	Clock Generation Unit
Class-AB	Class-AB headphone amplifier
DAC	Digital to Analog Converter
DAI	Digital Audio Input
DAO	Digital Audio Output
DMA	Direct Memory Access
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
INTC	INTerrupt Controller
IOCONF	Input Output CONFiguration
ISRAM	Internal RAM Memory
ISROM	Internal ROM memory
I^2C M/S	Inter IC Communication Master/Slave interface
JTAG	Joint Test Action Group
PHY	PHYsical layer
PLL	Phase Locked Loop
PSU	Power Supply Unit
SAI	Simple Audio Input
SAO	Simple Audio Output
SDAC	Stereo Digital to Analog Converter
SDMA	Simple Direct Memory Access controller
SysCReg	System Control Registers
Timer	Timer module
UART	Universal Asynchronous Receiver Transmitter
USB 2.0 FS	Universal Serial Bus 2.0 Full-Speed device
VPB	VSLI Peripheral Bus
VPB bridge	AHB to VPB bridge
VSLI	Very Large Scale Integration
Watchdog / WDOG	Watchdog timer

14. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PNX0161_1	20080117	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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